Write your name here. save this file as yournickname.v OR yournickname.vhd

clk, rst, card, Lin, vip, PA are input signals
Lout, PL1 and PL2 are output signals
clk is the master clock = 20 MHz = 50 ns
rst is master reset
card is card input, card = 1 means the presence of a card
Lin is load input signal, assume maximum load input is P500.

In your test bench initialize Lin = 50, vip = 1 if user is a VIP. Initialize vip = 1. When Lin < 13, Change to vip = 0 and add 40 to Lin. PA = 1 means to play again. In your test bench initialize PA = 1. Lout is the new load value. In your test bench, equate Lin to Lout.

At S4, PL1 = a 150 ns high pulse, at S6, PL2 = a 100 ns high pulse

S0: Initialize all signals here. Optional: if rst = 0, remain at S0. If there is a card go to S1 else remain in S0.

To get a grade of A = 100, implement the fsm below using a fully synchronous synthesizable code with a testbench that traverses all states. State transition occurs every 250 ns