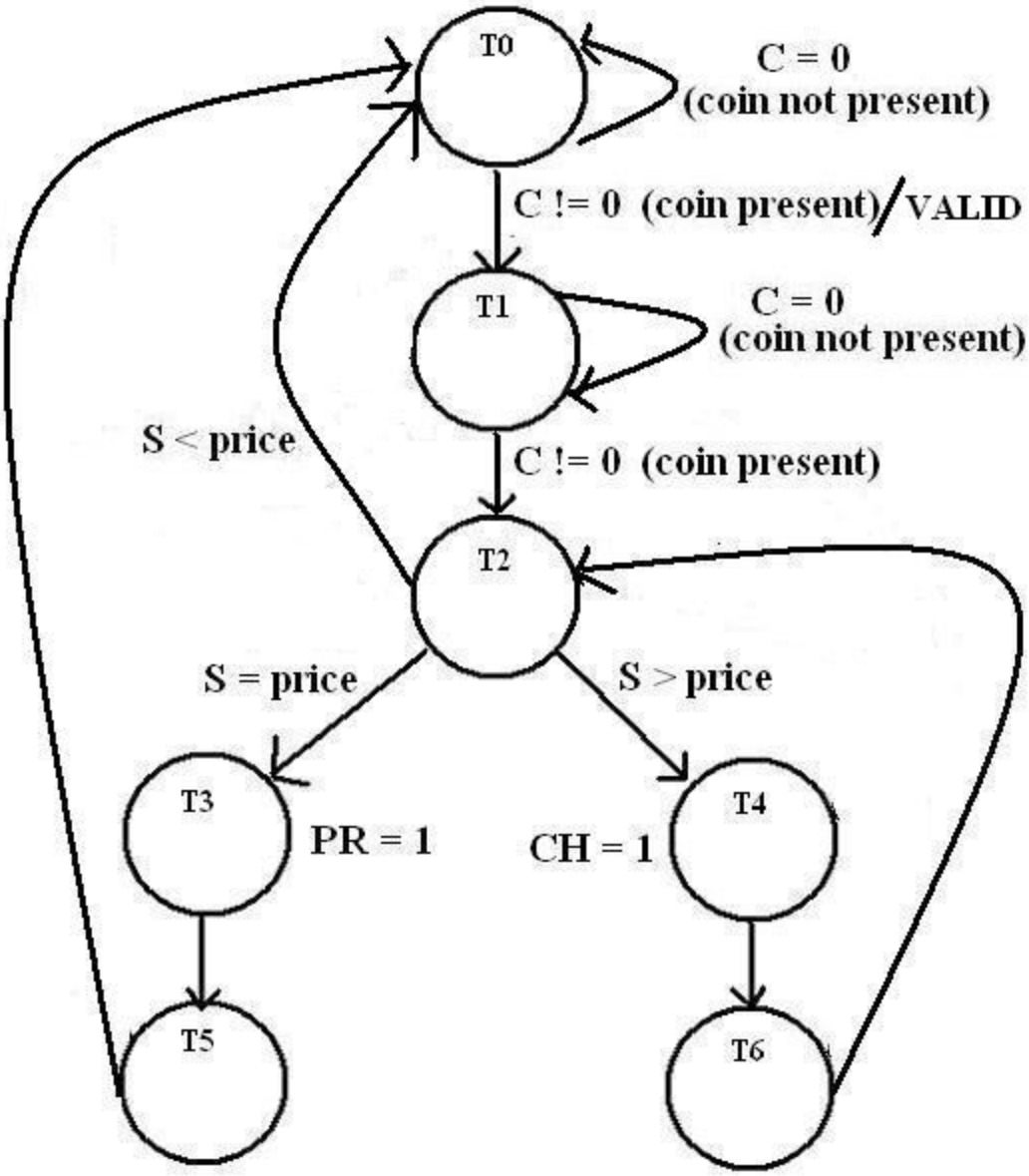
Write the verilog program for the given finite state machine. Write the corresponding testbench that will traverse all states, in particular write a testbench with stream input of C = 1, C = 5, C = 10 then C = 10. Let price = 20 pesos.

Definition and state actions:
module my_name(RST, CLK, C, S, STATE, VALID, PR, CH);
CLK : master clock, assume that the period is 20 ns.
RST : master reset.
Where C is an input. Price is a parameter initially set to 18. S, STATE, VALID, PR & CH are outputs.

Transition from one state to another occurs every 120 ns.



T0 : reset & initialization state, coin validation. Reset and initialize all signals here. Coin is validated here, if not valid C value is set to 0 (as if no coin is inserted). In this state, you are to activate a signal called VALID when a coin is inserted and validated to have a correct value (i.e. 1, 5 or 10). VALID is needed by the coin releaser device.. If VALID = 1 for 20 ns to 120 ns, the coin will be directed to the validated coin bin else it will be returned. For an A, set VALID = 40 ns :-).

T1 : coin amount detection state. C = coin value. When there is no validated coin present or inserted in the vendo machine, C = 0. If a coin is inserted and validated, assume that the coin will have one of these values C = 1 (one peso), C = 5 (five pesos) or C = 10 (ten pesos).

T2 : Amount determination state. Assume that there is only one product whose price is P17 (set this using your testbench since price is an input signal). S = sum or total amount inserted in the vendo machine.

T3 : Product release state. Assume you have a product releasing device. In this state, you are to activate a signal called PR = product release signal. PR is the signal needed by the product releasing device. If PR = 1 for 20 ns to 120 ns, 1 product will be released. For an A, set PR = 1 for 60 ns :-).

T5 : Reset Sum state. Here the accumulator S will be reset to 0.

T4 : Coin changer state. Assume that you have a coin changer device. This coin changer device releases one peso coin per signal CH = coin changer release signal. In this state, you are to activate a signal called CH = coin changer release signal. CH is the signal needed by the P1-coin releasing device. If CH = 1 for 20 ns to 120 ns, one P1-coin will be released. For an A, set CH = 1 for 80 ns :-).

T6 : Sum decrement state. In this state S is decremented by 1 (S = S -1).

Grading System:

98 to 100 : Working design ☺. Fully synchronous and synthesizable design, excellent testbench ☺.

95 to 97 : Working design ☺. Fully synchronous and synthesizable design, minimum testbench requirement.

92 to 94 : Working design ☺. Fully synthesizable design, minimum testbench requirement.

86 to 91 : Working design ☺. No #delay commands in design, minimum testbench requirement.

75 to 85 : Working design ☺. Minimum testbench requirement.

Else 0 to 74.