DESIGN OF A SYNTHESIZABLE MC6502-BASED μP USING VERILOG HDL

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Abstract

The implementation of a synthesizable 8-bit MC6502-based microprocessor using Verilog HDL includes 56 instructions available in 13 addressing modes, the exact number of clock cycles used to execute each instruction, interrupt capability, and an assembler that converts a user program written in assembly language to machine code. The design was tested and verified through simulations and by downloading the design into a Field-Programmable Gate Array (FPGA). An extensive testbench was created for each instruction to test the functionality of the design, and the results agree with expected values. Sample programs were successfully implemented in the FPGA as well. This project could serve as a springboard for research applications of the MC6502-based microprocessor and a cornerstone for designing other microprocessor systems.